

FORM PTO-1390 (Modified) (REV 11-98)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER 112740-147	
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371				U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 09/762517)	
INTERNATIONAL APPLICATION NO. PCT/DE99/02130		INTERNATIONAL FILING DATE July 9, 1999		PRIORITY DATE CLAIMED August 3, 1998	
TITLE OF INVENTION INTEGRATED CIRCUIT WITH BUILT-IN MODULE TEST					
APPLICANT(S) FOR DO/EO/US Franz HUTNER					

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

- ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
- ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
- ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
- ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
- ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
 - ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
 - ☒ has been transmitted by the International Bureau.
 - ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
- ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
- ☐ A copy of the International Search Report (PCT/ISA/210).
- ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
 - ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
 - ☐ have been transmitted by the International Bureau.
 - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - ☒ have not been made and will not be made.
- ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
- ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
- ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
- ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

- ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
- ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
- ☒ A **FIRST** preliminary amendment.
- ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
- ☐ A substitute specification.
- ☐ A change of power of attorney and/or address letter.
- ☒ Certificate of Mailing by Express Mail
- ☒ Other items or information:

Submission of Drawings Form;
Drawings (4 sheets)

U.S. APPLICATION NO. (IF KNOWN) SEE 37 CFR <div style="font-size: 2em; font-weight: bold; margin-top: 5px;">09/762517</div>	INTERNATIONAL APPLICATION NO. <div style="font-weight: bold; margin-top: 5px;">PCT/DE99/02130</div>	ATTORNEY'S DOCKET NUMBER <div style="font-weight: bold; margin-top: 5px;">112740-147</div>
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21. The following fees are submitted: BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :				CALCULATIONS PTO USE ONLY	
<input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO \$1,000.00					
<input checked="" type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO \$860.00					
<input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$710.00					
<input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$690.00					
<input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00					
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$860.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				\$0.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	9 - 20 =	0	x \$18.00	\$0.00	
Independent claims	1 - 3 =	0	x \$78.00	\$0.00	
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>				\$0.00	
TOTAL OF ABOVE CALCULATIONS =				\$860.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable) <input type="checkbox"/>				\$0.00	
SUBTOTAL =				\$860.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).				\$0.00	
TOTAL NATIONAL FEE =				\$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable) <input type="checkbox"/>				\$0.00	
TOTAL FEES ENCLOSED =				\$860.00	
				Amount to be refunded	\$
				charged	\$

☒ A check in the amount of **\$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees.
 A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **02-1818** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO: <div style="border: 1px solid black; padding: 5px;"> William E. Vaughan, Esq. Bell, Boyd & Lloyd LLC P.O. Box 1135 Chicago, Illinois 60690-1135 Tel: (312) 807-4292 </div>	<div style="text-align: center;"> SIGNATURE </div> <div style="text-align: center;"> Robert M. Barrett NAME </div> <div style="text-align: center;"> 30,142 REGISTRATION NUMBER </div> <div style="text-align: center;"> February 5, 2001 DATE </div>
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BOX PCT

IN THE UNITED STATES ELECTED/DESIGNATED OFFICE
 OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
 UNDER THE PATENT COOPERATION TREATY-CHAPTER II

5

PRELIMINARY AMENDMENT

APPLICANT: Franz Hutner DOCKET NO: 112740-147
 SERIAL NO: GROUP ART UNIT:
 EXAMINER:
 INTERNATIONAL APPLICATION NO: PCT/DE99/02130
 INTERNATIONAL FILING DATE: 09 July 1999
 INVENTION: INTEGRATED CIRCUIT WITH BUILT-IN MODULE TEST

15 Assistant Commissioner for Patents,
 Washington, D.C. 20231

Sir:

20 Please amend the above-identified International Application before entry
 into the National stage before the U.S. Patent and Trademark Office under 35 U.S.C.
 §371 as follows:

In The Specification:

On page 1, cancel lines 1-4 and substitute the following therefor:

--SPECIFICATION

25

TITLE**INTEGRATED CIRCUIT WITH BUILT-IN MODULE TEST****BACKGROUND OF THE INVENTION****Field of the Invention--.**

On page 1, line 5, insert --present-- before "invention".

30 On page 1, line 5, insert --, generally,-- after "relates".

On page 1, line 6, cancel "especially" and substitute therefor --, more
 particularly,--.

On page 1, line 8, cancel "self test" and substitute therefor --self-test--.

On page 1, before line 9, insert the following left-hand justified heading:

--Description of the Prior Art--

On page 1, line 10, cancel "self test" and substitute therefor --self-test--.

5 On page 1, line 10, cancel "by means of" and substitute therefor --via--.

On page 1, line 22, insert --are-- before "not".

On page 1, line 29, insert a --,-- after "etc.".

On page 2, line 4, insert a --,-- after "faults".

On page 2, line 4, cancel "did" and substitute therefor --does--.

10 On page 2, line 7, cancel "consists in that" and substitute therefor --is one
by which--.

On page 2, line 13, cancel "only".

On page 2, cancel lines 15-21 and substitute the following therefor:

15 --The present is, thus, directed to the development of an integrated circuit
wherein the costs for testing a module can be considerably reduced.

SUMMARY OF THE INVENTION--

On page 2, line 22, cancel "According to the invention, the" and substitute
therefor --Accordingly, a--.

On page 2, line 23, insert --of the present invention-- before "is".

20 On page 2, line 23, cancel "thus".

On page 2, line 29, cancel "also".

On page 2, line 30, insert a --,-- after "circuit".

On page 3, line 6, insert a --,-- after "vectors".

On page 3, line 6, insert --it has-- after "and".

25 On page 3, line 15, cancel the "," and substitute therefor a --;--.

On page 3, line 27, cancel "circuit" after "internal".

On page 3, line 27, cancel "the" after "and".

On page 3, line 27, cancel "circuit" after "external" and substitute therefor
--circuits--.

10/03/2020 10:00:00

On page 3, line 27, cancel "is".

On page 3, line 27, insert --is-- after "also".

On page 3, line 28, cancel "makes it possible to reduce" and substitute therefor --enables a reduction in--.

5 On page 3, line 31, insert --of the present invention-- after "embodiment".

On page 3, line 34, cancel ", as" and substitute therefor --. As--.

On page 3, line 34, insert a --,-- after "result".

On page 3, line 34, cancel "of which".

On page 4, line 1, cancel "can".

10 On page 4, line 1, insert --can-- after "also".

On page 4, line 5, insert a --,-- after "of".

On page 4, line 5, insert a --,-- after "to" and before "the".

On page 4, line 7, cancel "further" and substitute therefor --another--.

On page 4, line 8, insert --of the present invention-- after "embodiment".

15 On page 4, line 10, cancel the ",," and substitute therefor a --;--.

On page 4, cancel lines 18-20 and substitute the following therefor:

--Additional features and advantages of the present invention are described in, and will be apparent from, the following Detailed Description of the Preferred Embodiments and the Drawings.

20 **DESCRIPTION OF THE DRAWINGS--.**

On page 4, line 22, insert --of the present invention-- after "embodiment".

On page 4, line 24, cancel "diagrammatic".

On page 4, line 26, cancel "diagrammatic".

On page 4, line 28, insert --schematic-- before "representation".

25 On page 5, line 2, insert --of the present invention-- after "embodiment".

On page 5, line 5, cancel "representation" and substitute therefor --timing diagram--.

On page 5, before line 11, insert the following centered heading:

--DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS--.

On page 5, line 12, insert --of the present invention-- after “embodiment”.

On page 5, line 13, cancel “comprising” and substitute therefor --including--.

On page 5, line 21, cancel “usually”.

5 On page 5, line 28, cancel “essentially exhibits” and substitute therefor --includes--.

On page 5, line 30, cancel “diagrammatic”.

On page 6, line 2, cancel “multiplicity” and substitute therefor --plurality--.

On page 6, line 3, insert --wherein-- after the “,”.

10 On page 6, line 4, cancel “being” and substitute therefor --is--.

On page 6, line 11, insert a --,-- after “is”.

On page 6, line 11, insert a --,-- after “case”.

On page 6, line 23, cancel “diagrammatic”.

On page 6, line 25, cancel “figure” and substitute therefor --Figure--.

15 On page 6, line 31, cancel “figure” and substitute therefor --Figure--.

On page 6, line 32, cancel “multiplicity” and substitute therefor --plurality--.

On page 6, line 33, insert a --,-- after “and”.

On page 6, line 33, insert a --,-- after “again”.

20 On page 6, line 33, cancel “exhibits” and substitute therefor --includes--.

On page 7, line 3, cancel “in”.

On page 7, line 3, cancel “a manner”.

On page 7, line 14, cancel “figures” and substitute therefor --Figures--.

On page 7, line 17, cancel “, respectively,”.

25 On page 7, line 18, cancel “can”.

On page 7, line 18, insert --can-- after “also”.

On page 7, line 20, cancel “The” and substitute therefor --A--.

On page 7, line 21, cancel “lies in” and substitute therefor --is--.

On page 7, line 23, cancel “additionally” and substitute therefor --also--.

On page 10, line 25, insert --logic 2-- after “internal”.

On page 10, line 25, cancel “logic” and substitute therefor --circuit 14--.

On page 10, line 28, insert --of the present invention-- after “embodiment”.

On page 10, line 29, cancel “where” and substitute therefor --wherein--.

5 On page 11, line 7, cancel “figure” and substitute therefor --Figure--.

On page 11, include the paragraph which begins on line 8 in the paragraph which ends on line 7.

On page 11, line 11, insert --present-- before “invention”.

On page 11, line 20, cancel “is”.

10 On page 11, line 20, insert --is-- after “also”.

On page 11, line 22, cancel “by means of” and substitute therefor --via--.

On page 11, line 25, cancel “figure” and substitute therefor --Figure--.

On page 12, line 2, insert --present-- before “invention”.

On page 12, line 11, cancel “figure” and substitute therefor --Figure--.

15 On page 12, line 19, cancel “logic” and substitute therefor --circuit--.

On page 12, line 26, insert --present-- before “invention”.

On page 12, line 32, insert a --,-- after “can”.

On page 12, line 32, insert a --,-- after “therefore”.

On page 13, line 1, cancel “which presents” and substitute therefor --to
20 prevent--.

On page 13, line 8, cancel “by means of” and substitute therefor --with regard to--.

On page 13, line 13, cancel “thus”.

On page 13, line 15, cancel “as” and substitute therefor --. As--.

25 On page 13, line 15, insert a --,-- after “result”.

On page 13, line 15, cancel “of which”.

On page 13, line 16, cancel “of” after “or”.

On page 13, after line 18, insert the following paragraph:

--Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.--

5 On page 17 (last page), cancel lines 1-3 and substitute the following centered heading therefor::

--ABSTRACT OF THE DISCLOSURE--

On page 17, line 5, insert --present-- before 'invention'.

On page 17, line 6, cancel "(1)".

10 On page 17, line 6, cancel "especially" and substitute therefor -- particularly--.

On page 17, line 7, cancel "multiplicity" and substitute therefor -- plurality--.

On page 17, line 7, cancel "(2)".

15 On page 17, line 7, cancel ". To" and substitute therefor --, wherein to--.

On page 17, line 8, cancel "multiplicity" and substitute therefor -- plurality--.

On page 17, line 8, cancel "(2)".

On page 17, line 9, cancel "(3)".

20 On page 17, line 10, cancel "(4)".

On page 17, line 10, cancel "(5)." and substitute therefor a --;--.

On page 17, line 11, cancel "In addition,".

On page 17, line 11, cancel "(14, 15)" and substitute therefor --also--.

On page 17, line 12, cancel "(3)".

25 On page 17, line 13, cancel "(7)".

On page 17, line 14, insert --as well-- after "circuit".

On page 17, cancel line 16.

30

In the Claims:

On page 14, cancel line 1, and substitute the following left-hand justified heading therefor:

--I Claim As My Invention:--

5 Please cancel claims 1-9, without prejudice, and substitute the following claims therefor:

10. An integrated circuit, comprising:

a plurality of logic gates for implementing a logic function of the integrated circuit; and

10 a self-test circuit for performing an internal self test of the plurality of logic gates, the self-test circuit including a test pattern generator for generating a test pattern, a test response analyzer for evaluating a test response, and an input/output circuit via which the self-test circuit further performs a logic test of an external circuit, the self-test circuit testing both the plurality of logic gates and the external
15 circuit at the same time, wherein a first part of the test pattern is supplied to the plurality of logic gates and a second part of the test pattern is supplied to the external circuit via the input/output circuit, and the test response is produced from a first part of the test response from the plurality of logic gates and a second part of the test response from the external logic circuit.

20

11. An integrated circuit as claimed in claim 10, wherein both the test pattern generator and the test response analyzer are linear-feedback shifted registers.

25

12. An integrated circuit as claimed in claim 10, wherein the test pattern generator generates pseudo-random vectors as the test pattern.

13. An integrated circuit as claimed in claim 10, wherein the input/output circuit includes input/output drivers for sending and receiving
30 unidirectional signals between the self-test circuit and the external circuit.

14. An integrated circuit as claimed in claim 10, wherein the input/output circuit includes controllable input/output drivers for sending and receiving bidirectional signals between the self-test circuit and the external circuit, and wherein the self-test circuit further includes a control device which controls the controllable input/output drivers.

15. An integrated circuit as claimed in claim 14, wherein the control device controls both the self-test circuit and the output circuit such that an initialization of the external circuit is performed in a first test cycle and the self test of the plurality of logic gates and the logic test of the external circuit are performed in a second test cycle.

16. An integrated circuit as claimed in claim 14, wherein the input/output circuit includes a bus connection for connecting to an external bus structure and the control device includes a bus control, wherein external circuit elements connected to the bus structure are selectively selected for a self-test via respective enable signals.

17. An integrated circuit as claimed in claim 16, wherein the bus control includes a counter for counting a bus clock signal, wherein the controllable input/output drivers are only selected during all even-numbered clock cycles of the bus clock signal and the respective enable signals are output sequentially during all odd-numbered clock signals of the bus clock signal for enabling the respective external circuit elements.

18. An integrated circuit as claimed in claim 10, wherein the input/output circuit can be selectively deactivated.

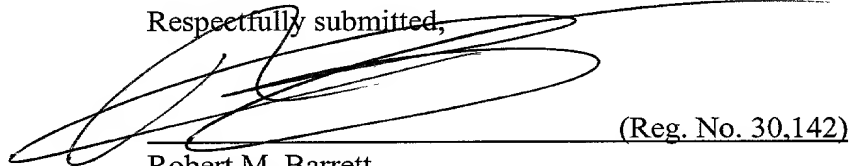
REMARKS

The present amendment makes editorial changes and corrects typographical errors in the specification in order to conform the specification to the requirements of the United States Patent practice. No new matter is added thereby. Original
5 claims 1-9 have been canceled in favor of new claims 10-18. Claims 10-18 have been presented solely because the revisions by bracketing and underlining which would have been necessary in claims 1-9 in order to present those claims in accordance with preferred United States Patent practice would have been too extensive, and thus would have been too burdensome. The amendment is intended
10 for clarification purposes only and not for substantial reasons related to patentability pursuant to 35 U.S.C. §§101, 102, 103 or 112. Indeed, the cancellation of claims 1-9 does not constitute an intent on the part of the Applicant to surrender any of the subject matter of claims 1-9.

Early consideration on the merits is respectfully requested.

15

Respectfully submitted,



(Reg. No. 30,142)

20

Robert M. Barrett
Bell, Boyd & Lloyd LLC
P.O. Box 1135
Chicago, Illinois 60690-1135
(312) 807-4042
Attorneys for Applicant

PCT

WELTORGANISATION FÜR GEISTIGES EIGENTUM
Internationales Büro



INTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE
INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

(51) Internationale Patentklassifikation 7 : G01R 31/3185	A1	(11) Internationale Veröffentlichungsnummer: WO 00/08479 (43) Internationales Veröffentlichungsdatum: 17. Februar 2000 (17.02.00)
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(21) Internationales Aktenzeichen: PCT/DE99/02130
(22) Internationales Anmeldedatum: 9. Juli 1999 (09.07.99)
(30) Prioritätsdaten:
198 34 976.9 3. August 1998 (03.08.98) DE
(71) Anmelder (für alle Bestimmungsstaaten ausser US): SIEMENS
AKTIENGESELLSCHAFT [DE/DE]; Wittelsbacherplatz 2,
D-80333 München (DE).
(72) Erfinder; und
(75) Erfinder/Anmelder (nur für US): HUTNER, Franz [DE/DE];
Bruckerstrasse 2, D-85254 Einsbach (DE).
(74) Gemeinsamer Vertreter: SIEMENS AKTIENGE-
SELLSCHAFT; Postfach 22 16 34, D-80506 München
(DE).

(81) Bestimmungsstaaten: CN, DE, ID, US.

Veröffentlicht

Mit internationalem Recherchenbericht.
Vor Ablauf der für Änderungen der Ansprüche zugelassenen
Frist; Veröffentlichung wird wiederholt falls Änderungen
eintreffen.

(54) Title: INTEGRATED CIRCUIT WITH AN INTEGRATED MODULE TEST

(54) Bezeichnung: INTEGRIERTE SCHALTUNG MIT EINGEBAUTEM BAUGRUPPENTEST

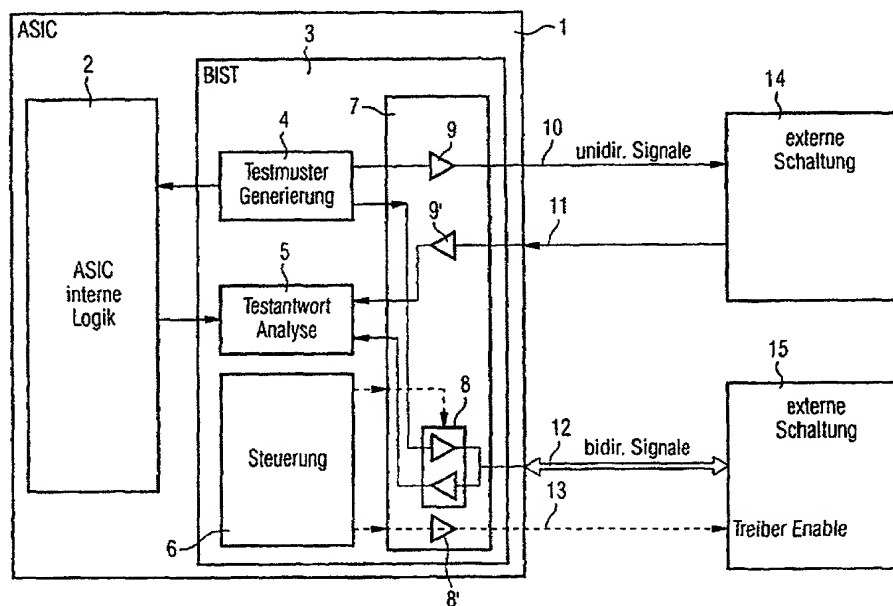
(57) Abstract

The invention relates to an integrated circuit (1), especially an ASIC, comprised of a plurality of logic gates (2). A self-test circuit (3) is provided for conducting an internal self-test of the plurality of logic gates (2). Said self-test circuit comprises a test pattern generator (4) and a test response analyzer (5). In addition, an input/output circuit (7) which is provided in the integrated circuit enables a test of an external circuit (14, 15) to be conducted with the self-test circuit (3), said self-test circuit being integrated in the integrated circuit.

(57) Zusammenfassung

Die Erfindung betrifft eine integrierte Schaltung (1), insbesondere ein ASIC, die aus einer Vielzahl von logischen Gattern (2) besteht. Zum Durchführen eines internen

Selbsttests der Vielzahl von logischen Gattern (2) ist eine Selbsttestschaltung (3) vorgesehen, die einen Testmuster-Generator (4) und einen Testantwort-Analysator (5) aufweist. Über eine in der integrierten Schaltung vorgesehene Ein-/Ausgangsschaltung (7) kann mit der in der integrierten Schaltung eingebauten Selbsttestschaltung (3) darüber hinaus ein Test einer externen Schaltung (14, 15) durchgeführt werden.



2...ASIC INTERNAL LOGIC
4...TEST PATTERN GENERATION
5...TEST RESPONSE ANALYSIS
6...CONTROL

10...UNIDIRECTIONAL SIGNALS
12...BIDIRECTIONAL SIGNALS
14...EXTERNAL CIRCUIT
15...DRIVER ENABLE

Description

Integrated circuit with built-in module test

5 The invention relates to an integrated circuit with built-in module test and especially to an application-specific integrated circuit (ASIC) with a built-in self test (BIST).

10 Many conventional integrated circuits already have a built-in self test (BIST) by means of which an internal check of the logic functions of the integrated circuit is performed with each new switch-on of the integrated circuit. This makes it possible to test
15 critical chips before any use in the system or, respectively, in a particular hardware environment. Integrated circuits with high complexity such as, for example, INTEL processors already have such a self-test circuit. However, these conventional built-in self-test
20 (BIST) circuits only check the internal logic of an integrated circuit. All output signals going to the outside or input signals present from outside are kept constant and/or not switched through in these circuits.

25 Although this makes it possible to check the respective integrated circuits in a simple and effective manner, a large proportion of the faults in a module or a board which, for example, result from faulty board connections, contact faults on the circuit board, poor soldering joints, defective I/O connections of the chips etc. remains undetected.

09/762517 05 FEB 2001

Such faults in a module are usually detected and localized in time-consuming board tests. In these tests, the partially equipped circuit boards are checked for faults but this did not achieve complete
5 testing of the boards.

Another conventional test of a completely configured system consists in that, with each restart, software test routines are initiated which functionally test the module or board. However, this method, too,
10 does not achieve complete testing of the board. Instead, a large proportion of the possible faults on a board remains undetected by this test which leads to failures with extremely high costs only when it is finally used.

15 The invention is, therefore, based on the object of developing an integrated circuit according to the preamble of claim 1 in such a manner that the costs for testing a module can be considerably reduced.

According to the invention, this object is
20 achieved by means of the features specified in the characterizing clause of claim 1.

According to the invention, the self-test circuit built into the integrated circuit is thus used not only for testing the internal logic but also for
25 testing the external logic located on the module. In this arrangement, in particular, the input/output connections of the integrated circuit are not kept constant but the test pattern generated in the self-test circuit is also output to the chips of the module
30 connected externally via an input/output circuit and a received test response of these

external chips is evaluated with the built-in self-test (BIST) circuit.

5 The self-test circuit preferably has a test pattern generator for generating a test pattern or, respectively, a signature in the form of pseudo-random vectors and a test response analyzer for evaluating the test response coming from the internal logic and/or external logic. By using test pattern generators and test response analyzers, which are already known, a
10 self-test circuit which tests both the internal logic and the external logic in the module can be implemented with minimum expenditure and with the smallest space requirement in the integrated circuit.

15 The internal logic and the external logic are preferably tested at the same time, a first section of the test pattern generated by the test pattern generator being output to the internal logic and a second section of the signature being output to the external circuit. Both the internal logic and the
20 external logic provide the respective sections, derived from the signature, of a test response which are compressed and evaluated in the common test response analyzer. The simultaneous testing of the internal and external circuit reduces, in particular, the time
25 expended for the test with each restart of the system. As an alternative, however, a time-sequential test of the internal circuit and the external circuit is also possible which makes it possible to reduce the area required by the self-test circuit in the integrated
30 circuit.

According to a preferred exemplary embodiment, the output circuit exhibits controllable input/output drivers for sending and receiving bidirectional signals, as a result of which the

integrated circuit can also be tested in a hardware environment which, for example, exhibits a bus structure. In particular, use of a control device which controls the drivers of the external components makes it possible to prevent destruction of or damage to the driver stages during the self test.

Furthermore, according to a further preferred exemplary embodiment, the control device of the self-test circuit can be designed in such a manner that two test runs are performed, the first test run being used for initializing undefined chip groups whereas the second test run corresponds to the actual test of the respective components. This makes it possible to also test components with undefined starting levels such as, for example, random-access memories (RAMs) since they are written to in a defined manner in the first test run and are only tested in the second test run.

In the text which follows, the invention will be described in greater detail by means of exemplary embodiments and referring to the drawing, in which:

Figure 1 shows a block diagram of a module according to a first preferred exemplary embodiment, with an integrated circuit and an external circuit;

Figure 2 shows a diagrammatic block diagram of a test pattern generator shown in Figure 1;

Figure 3 shows a diagrammatic block diagram of a test response analyzer shown in Figure 1;

Figure 4 is a representation for illustrating the division of a test pattern into a first part for the internal logic and a second part for the external circuit;

Figure 5 shows a block diagram of a module according to a second preferred exemplary embodiment, with an integrated circuit and an external circuit with bus structure;

5 Figure 6 is a representation of a bus clock signal of the bus structure shown in Figure 5 for illustrating the chip selection; and

Figure 7 is a block diagram of a random-access memory which can be used, for example, as external component
10 in the bus structure according to Figure 5.

Figure 1 shows a block diagram of a module according to a first preferred exemplary embodiment, comprising an integrated circuit 1, a first external circuit 14 and a second external circuit 15. In the
15 text which follows, the integrated circuit 1 is designated as ASIC 1 since it preferably consists of an application-specific integrated circuit (ASIC). Such integrated circuits are particularly suitable for the present invention since they are specially designed for
20 particular applications in which the hardware or, respectively, the external circuitry is usually specified exactly and is produced in high numbers as system board or module assembly.

The ASIC 1 has an internal logic 2 which
25 consists of a plurality of logic gates and implements the logic function of the ASIC 1. The reference number 3 designates a built-in self-test (BIST) circuit which essentially exhibits a test pattern generator 4 and a test response analyzer 5.

30 Figure 2 shows a diagrammatic block diagram of the test pattern generator 4. The test pattern generator 4 consists,

for example, of a linear-feedback shift register (LFSR). In this arrangement, a multiplicity of flip-flops 18 are series-connected, the output signal of the last flip-flop being fed back to the input of the first flip-flop. To generate pseudo-random vectors which are used as test pattern 16, they can be located between the respective flip-flop's XOR gates 19 which provide for an exclusive-OR combination of the output signal of a respective flip-flop 18 with the output signal of the last flip-flop. The signal resulting from this exclusive-OR combination is in each case supplied to the input of the following flip-flop. The outputs of the series-connected flip-flops 18 are used as output signal and supply a test pattern or, respectively, a test signature 16 which represents a pseudo-random vector which, with a number of n flip-flops, reproduces $2^n - 1$ states in an apparently random but repetitive sequence. Such a test pattern or, respectively, such a test signature 16 is eminently suitable for testing highly complex logic circuits since it exhibits an extremely high test severity with the appropriate length of testing.

Figure 3 shows a diagrammatic block diagram of the test response analyzer 5 belonging to the test pattern generator 4 according to figure 2, which is used for compressing and evaluating a test response. The test pattern 16 generated by the test pattern generator 4 is supplied to a circuit to be tested and then generates a test response 17 at its output connections. This test response 17 is supplied to the test response analyzer 5 which, according to figure 3, consists of a multiplicity of series-connected flip-flops 18 and again exhibits a linear-feedback shift register (LFSR). The

test response analyzer 5 is configured in a manner corresponding to the test pattern generator 4 and the circuit to be tested in such a manner that it suitably compresses the test response 17 sent out by the circuit to be tested and outputs an output signal corresponding to the tested logic functions of the circuit to be tested. On the basis of these output signals and with knowledge of the output signals to be expected, it is possible to achieve a sufficiently high test accuracy or severity for detecting errors in the circuit to be tested if the number of test patterns 16 is sufficiently large. The examples for the test pattern generator 4 and the test response analyzer 5 shown in figures 2 and 3 are only used for explaining the principle of generating suitable test patterns and evaluating corresponding test responses. Naturally, the test patterns and test responses, respectively, described above can also be generated and evaluated, respectively, in a different manner.

20 The special feature of the present invention lies in that a test pattern 16 generated by the test pattern generator 4 is output not only to the internal logic of the ASIC 1 but additionally to the output connections of the integrated circuit or ASIC 1 via an output circuit 7. In contrast to a conventional integrated circuit with built-in self test, in which the output and input connections of the chip are kept constant, at least a part of the test pattern 16 generated by the test pattern generator 4 is present at

25 the output connections of the integrated circuit 1 via output drivers 9 in the integrated circuit 1 according to the invention.

30

Figure 4 shows a representation for illustrating the division of the test pattern 16 into a first and second part for testing the internal logic 2 and the external logic 14. According to figure 4, the internal logic 2 of the ASIC 1 only consists of one AND gate 20. The external circuit 14 is constructed, for example, of an OR gate 21 and a flip-flop 22. This highly simplified representation of a module to be tested is intended to represent the operation of the ASIC according to the invention in the text which follows. Three test patterns (11, 01, 10) are needed for testing the logic function of the AND gate 20 in the internal logic 2 of the ASIC 1. The logic function of the AND gate 20 can be completely tested with such a test pattern. The OR gate 21 in the external circuit can be tested by three test patterns (01, 10, 00). It is sufficient to check the change in logic level at the output of the flip-flop 22 as a function of the clock signal for a minimum test of the flip-flop 22.

This results in the test pattern sequence (011, 001, 010, 1XX) shown in figure 4, by means of which a minimum test of the internal logic 2 and of the external circuit 14 can be performed. According to the invention, the test pattern generator 4 generates a corresponding test pattern, a first part TM1 of the test pattern 16 being supplied to the internal logic 2 or, respectively, the AND gate 20 whilst a second part TM2 of the test pattern 16 is supplied to the external circuit 14 or, respectively, the OR gate 21 via an output driver 9 and the output connection of the ASIC 1. The reference symbol TA1 here represents the test response of the internal logic 2 whilst TA2 is the test response of the external circuit 14 and is supplied to the test response analyzer 5 via an input driver 9'. The test response TA1 (1, 0, 0, X) output

by the internal logic 2 and the test response TA2 (1, 0, 0, 1) output by the external circuit 14 provide the complete test response 17 (11, 00, 00, X1) which is supplied to the test response analyzer 5 for evaluation. The signals analyzed by the test response analyzer 5 are compared with a signal sequence to be expected, and the test is successful or, respectively, there are no faults in the internal logic 2 and the external logic 14 if expected and received signal sequence match.

If the external circuit 14 consists of a purely combinatorial circuit, clock synchronism and/or defined resetting of the external components is not required. If, however, the external circuit 14 also consists of a sequential chip, i.e. clocked flip-flop 22 or the like, as shown in figure 4, all units included in the self test must operate in a clocked manner and be reset in a defined manner. In this arrangement, the ASIC 1 must have a connection which allows such defined resetting and clocked operation.

Figure 4 shows the ASIC 1 in conjunction with external, purely combinatorial and resettable sequential components which are connected to the ASIC 1 via unidirectional input/output signals 10/11. According to figure 1, an external circuit 15 which has combinatorial and/or sequential components can also communicate with the ASIC 1 via bidirectional signals 12. In this case, the input/output circuit 7 must have controllable input/output drivers 8 which enables the outgoing test patterns and incoming test responses to be separated in time. Such a control is implemented by a control device 6 which preferably controls

the input/output drivers 8 in the input/output circuit 7 in dependence on a clock signal of the bidirectional signals 12. In addition, the control device 6 must switch a driver enable signal via a driver stage 8' to an output connection of the ASIC 1 so that the driver enable signal 13 enables the driver of the external component at the correct time. With the exception of the transmission of the signature and the reception of the test response on one signal line being divided in time, the self test is performed in the same manner as described above.

In the self-test circuit 3 described above, it was assumed that the test pattern 16 generated by the test pattern generator 4 is divided and delivered to the internal logic and the external logic. In the same manner, however, it is also possible to divide the test pattern 16 generated by the test pattern generator 4 in time, the test pattern being transmitted completely to the internal logic 2 in a first time interval whereas it is delivered completely to the external circuit 14 or, respectively, 15 in a second time interval. Similarly, a self-test circuit is conceivable which consists of two test pattern generators and two test response analyzers which are in each case allocated to the internal and external logic. However, the operation corresponds to the operation described above.

Figure 5 shows a block diagram of a module according to a second preferred exemplary embodiment, where the ASIC 1 is connected to a bus structure 12' of the module or, respectively, board. At least one component connected to the bus structure 12' represents a component, the internal states of which cannot be brought to defined values by a reset signal. Such components

are, for example, random-access memories (RAMs) and the like.

Figure 7 shows a block diagram of a random-access memory 23 with its data inputs Din, address inputs ADR, its write enable input WE, its chip enable input CE and its data outputs Dout as can be used, for example, in the circuit according to figure 5.

Such storage chips, the internal states of which cannot be brought to a defined level by a reset signal, require separate treatment during the self test. According to the invention, the control device 6' of the ASIC 1 generates a separate test run before the actual self test until all states used in the external circuit and/or internal logic 2 are initialized. The actual self test is only performed after this initialization in which, for example, data are written into the RAM 23 in a defined manner. The test pattern 16 generated by the test pattern generator 5 can be used for the addressing and writing of the data for this initialization. However, it is also possible to use an initialization circuit which is independent of this and by means of which the respective components 23 are initialized before the actual self test.

A further problem of the bus structure shown in figure 5 is a driver conflict occurring between the components 23. With the currently used CMOS drivers of the chips, such a driver conflict must be avoided in order to prevent damage. However, since a pseudo-random stimulation is normally applied to all

signals and test patterns in the self test according to the invention, a bus conflict must be expected with such random actuation of a respective driver enable signal. To prevent this problem, a chip must drive its
5 output only every $2 \times n$ th clock pulse with n chips connected to a bus structure 12'.

Figure 6 shows a timing diagram of a bus clock signal for illustrating the conflict-free selection of a multiplicity of chips in a bus structure. In the case
10 of the external circuit with two external chips 23 shown in figure 5, the ASIC 1 only drives with clock pulses 0, 6, 12, Chip ① only drives its output in clock pulses 2, 8, 14, ... whereas chip ② only drives its output in clock pulses 4, 10, 16, All odd
15 clock pulses remain free in order to avoid bus conflicts between the disconnecting driver and the beginning driver. For this method, the driver control signal 13' must be accessible for enabling the respective chip 23 of the external logic. This means
20 that the ASIC 1 may have to exhibit additional output connections in order to supply the driver enable signal 13' to the external circuit under control of the control device 6'.

A further problem may arise in the case where a
25 module has a number of ASICs or integrated circuits 1, respectively, according to the invention. In this case, a number of integrated circuits would attempt to perform a self test of the external circuit. However, this would lead either to falsified test results or
30 even cause damage to the driver stages in the respective components. To solve this problem, the input/output circuit can therefore be selectively deactivated

which prevents the performance of an external test. This means that the test patterns are not sent to the external circuit via the input/output drivers 8 and 9, respectively, and the output connections of the chip as
5 a result of which the chip behaves like a conventional integrated circuit with built-in self test.

The present invention has been described, in particular, by means of an application-specific integrated circuit 1 (ASIC) since such a circuit is
10 particularly tailored to the respective requirements of a closely delimited application. Knowing this application or, respectively, the module in which the ASIC 1 is to be used, it is thus possible also to implement a self test for the external circuit in a
15 simple manner as a result of which a self test is performed with each restart of a module or of a hardware module and a complete board is tested in an extremely simple and inexpensive manner.

Patent claims

1. An integrated circuit comprising a multiplicity of logic gates (2) for implementing a logic function of the integrated circuit (1), and a self-test circuit (3) for performing an internal self test of the multiplicity of logic gates (2), the self-test circuit (3) exhibiting a test pattern generator (4) for generating a test pattern (16), a test response analyzer (5) for evaluating a test response (17) and an input/output circuit (7) by means of which the self-test circuit (3) performs a logic test of an external circuit (14, 15), characterized in that the multiplicity of logic gates (2) and the external circuit (14, 15; 23) are tested at the same time, a first part (TM1) of the test pattern (16) being supplied to the multiplicity of logic gates (2) and a second part (TM2) being supplied to the external circuit (14, 15; 23) via the input/output circuit (7) whereas the test response (17) is produced from a first part of response signals (TA1) of the multiplicity of logic gates (2) and from a second part of response signals (TA2) of the external logic circuit (14, 15; 23).
2. The integrated circuit as claimed in claim 1, characterized in that the test pattern generator (4) and the test response analyzer (5) consist of linear-feedback shift registers.
3. The integrated circuit as claimed in claim 1 or 2, characterized in that

the test pattern generator (4) generates pseudo-random vectors as test pattern.

4. The integrated circuit as claimed in one of claims 1 to 3, characterized in that the input/output circuit (7) exhibits input/output drivers (9, 9') for sending and receiving unidirectional signals (10, 11) between the self-test circuit (3) and the external circuit (14).

5. The integrated circuit as claimed in one of claims 1 to 4, characterized in that the input/output circuit (7) exhibits controllable input/output drivers (8) for sending and receiving bidirectional signals (12) between the self-test circuit (3) and the external circuit (15), a control device (6) controlling the drivers of the output circuit (7) and of the external circuit (15).

6. The integrated circuit as claimed in claim 5, characterized in that the control device (6) controls the self-test circuit (3) and the output circuit (7) in such a manner that an initialization of the external circuit (15; 23) is performed in a first test cycle and the self test of the multiplicity of logic gates (2) and of the external circuit (15) is performed in a second test cycle.

7. The integrated circuit as claimed in claim 5 or 6, characterized in that

the input/output circuit (7) exhibits a bus connection for connecting to an external bus structure (12') and the control device exhibits a bus control (6'), external circuit elements (23) connected to the bus structure (12') being selectively selected for a self test via respective enable signals (13').

8. The integrated circuit as claimed in claim 7, characterized in that the bus control (6') exhibits a counter for counting a bus clock signal, the controllable output drivers (8) only being selected during all even-numbered clock cycles of the bus clock signal and the respective enable signals (13') being output sequentially during all odd-numbered clock cycles of the bus clock signal for enabling the respective external circuit elements (23).

9. The integrated circuit as claimed in one of claims 1 to 8, characterized in that the input/output circuit (7) can be selectively deactivated.

Abstract

Integrated circuit with built-in module test

The invention relates to an integrated circuit (1), especially an ASIC, which consists of a multiplicity of logic gates (2). To perform an internal self test of the multiplicity of logic gates (2), a self-test circuit (3) is provided which exhibits a test pattern generator (4) and a test response analyzer (5). In addition, a test of an external circuit (14, 15) can be performed with the self-test circuit (3) built into the integrated circuit via an input/output circuit (7) provided in the integrated circuit.

Figure 1

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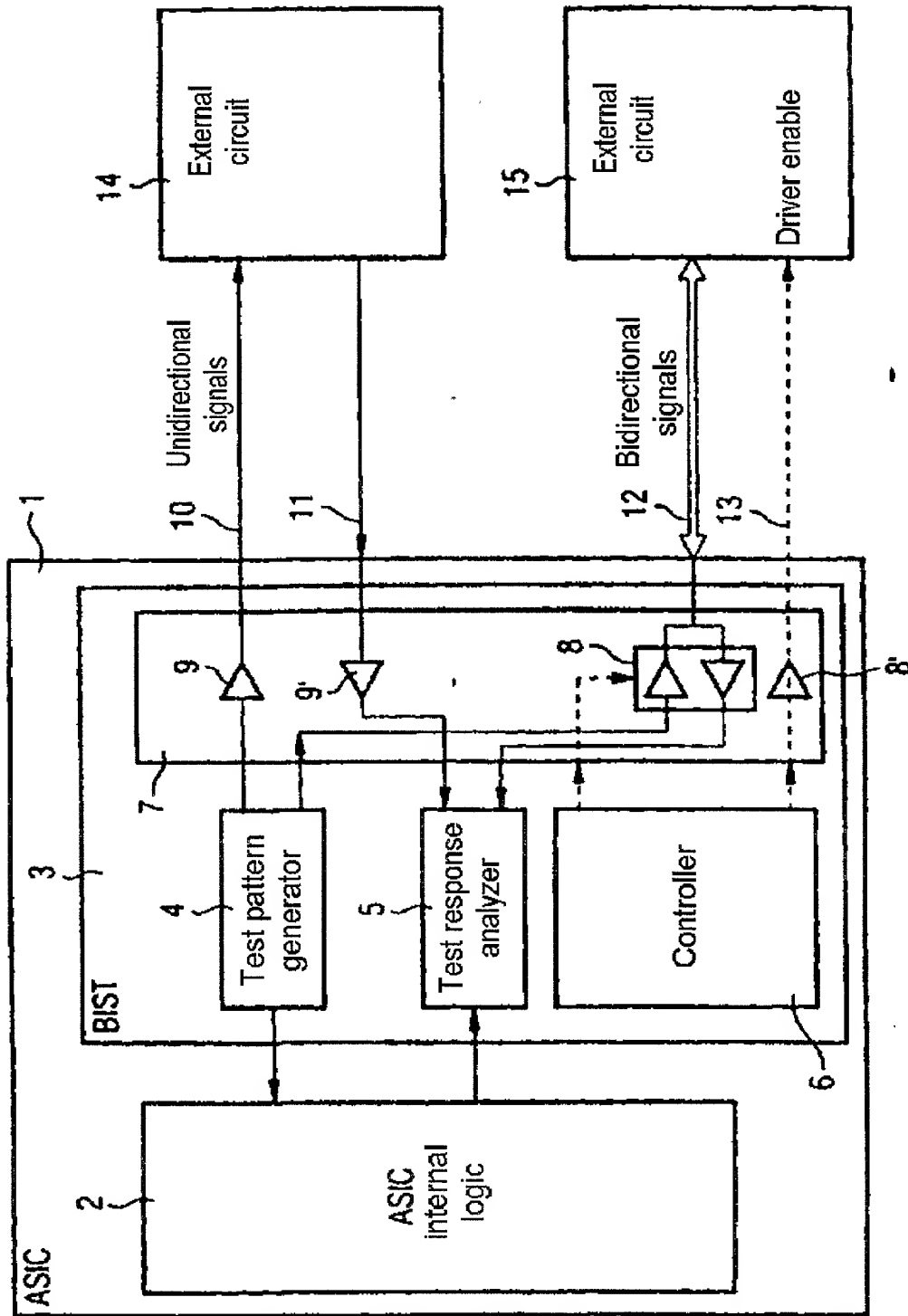


FIG 2

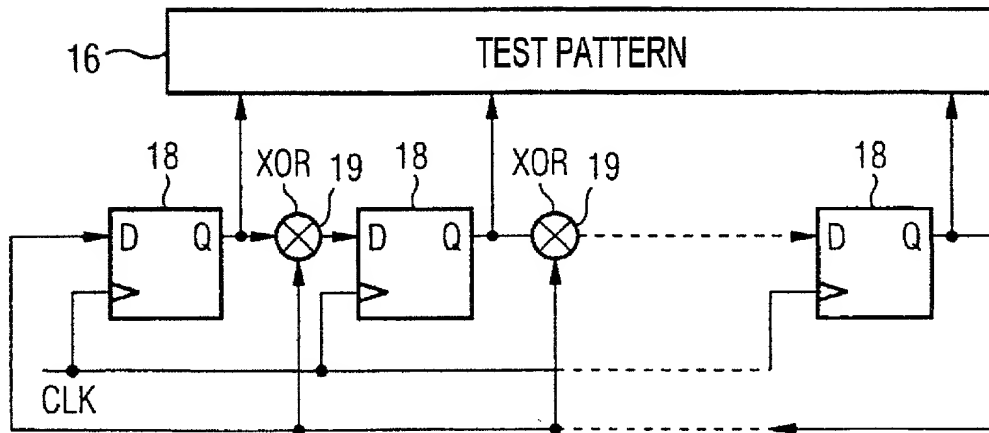
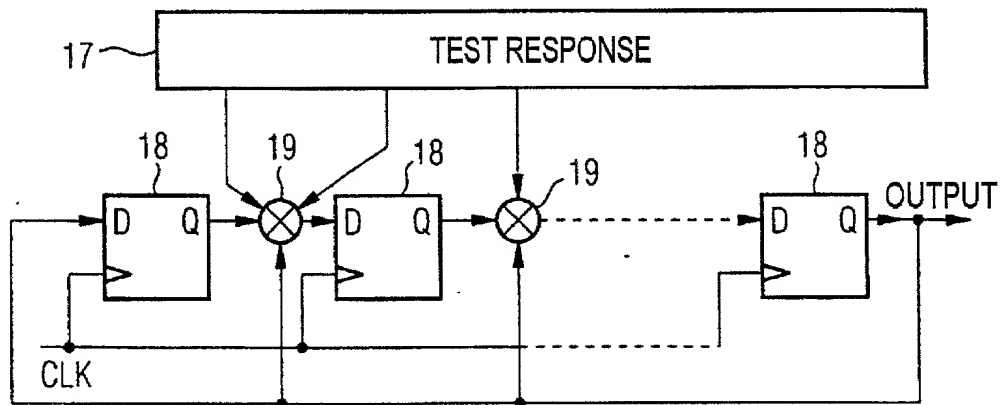


FIG 3



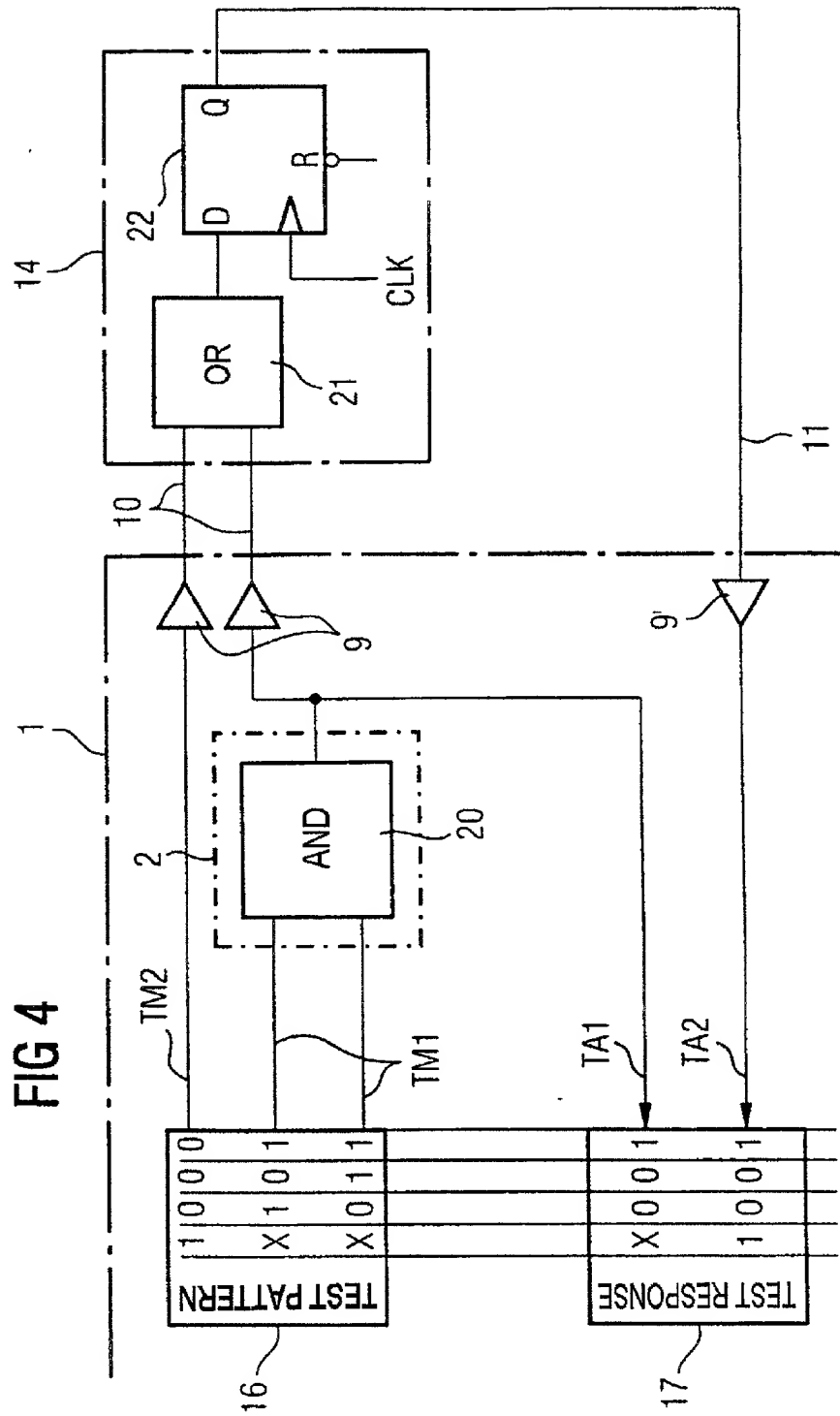


FIG 5

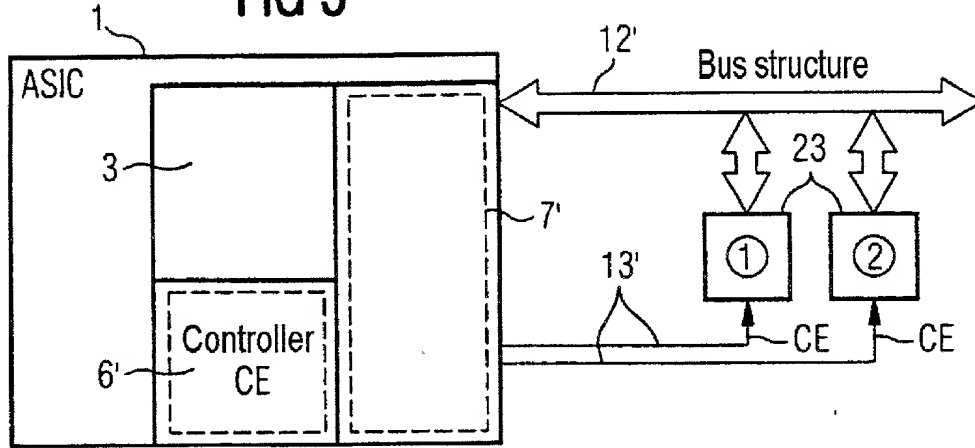


FIG 6

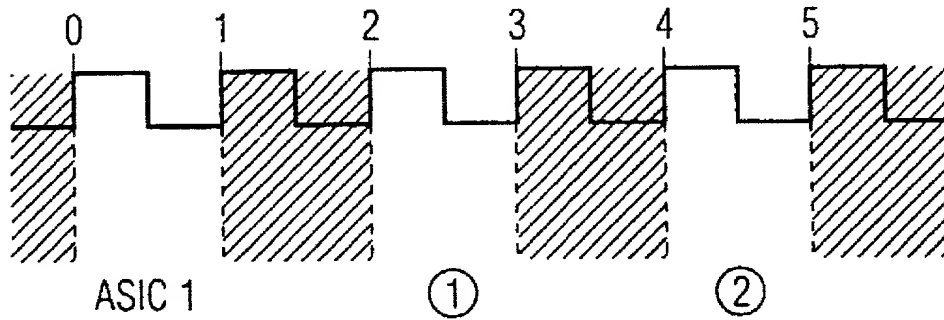
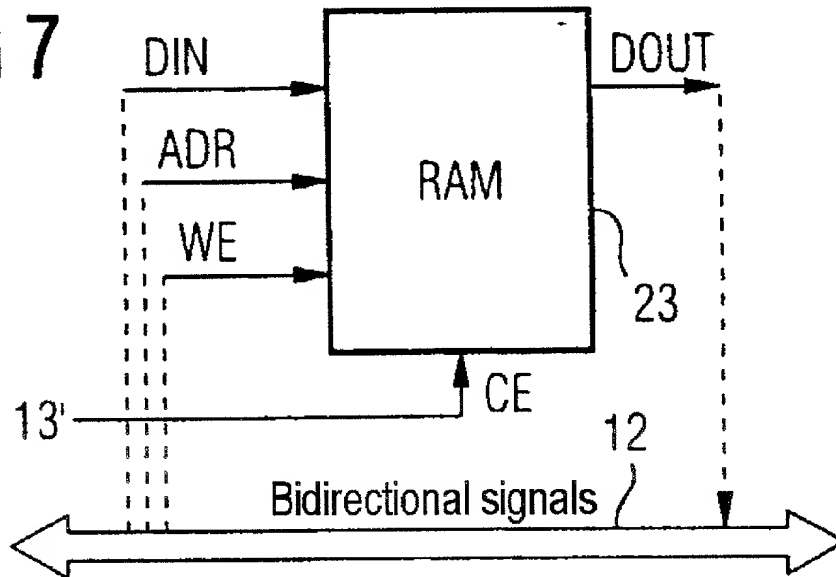


FIG 7



COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

(Includes Reference to PCT International Applications) PCT/DE99/02130

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As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTEGRATED CIRCUIT WITH BUILT-IN MODULE TEST

the specification of which (check only one item below):

☐ is attached hereto.☒ was filed as United States application
Serial No. 09/762,517on February 5, 2001

and was amended

on _____ (if applicable).

☐ was filed as PCT international application

Number _____

on _____

and was amended under PCT Article 19

on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

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COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
Germany	198 34 976.9	3 August 1998	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO

Combined Declaration For Patent Application and Power of Attorney (Continued) (Includes Reference to PCT International Applications) PCT/DE99/02130				ATTORNEY'S DOCKET NO. 112740-147	
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PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)			
POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) Holby M. Abern (P47,372), Robert M. Barrett (30,142), Alan L. Barry (30,819), Thomas C. Basso (46,541), Jeffrey H. Canfield (38,404), Robert W. Connors (46,639), Amy J. Gast (41,773), Timothy L. Harney (38,174), Patricia A. Kane (46,446), Michael S. Leonard (37,557), Edward A. Lehman (22,312), Adam H. Masia (35,602), Dante J. Picciano (33,543), Renato L. Smith (45,117), Maurice E. Teixeira (45,646), William E. Vaughan (39,056), Austin Victor (47,154), and all members of the firm of Bell, Boyd & Lloyd LLC.					
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BELL BOYD & LLOYD LLC P.O. Box 1135 Chicago, Illinois 60690				312/807-4292	
100 2 0 1	FULL NAME OF INVENTOR	FAMILY NAME HUTNER	FIRST GIVEN NAME FRANZ	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY D-85254 Einsbach <i>DEX</i>	STATE OR FOREIGN COUNTRY Germany	COUNTRY OF CITIZENSHIP Germany	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS Bruckerstrasse 2	CITY D-85254 Einsbach	STATE & ZIP CODE/COUNTRY Germany	
2 0 2	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY	
2 0 3	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP	
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DATE <i>17.04.2001</i>		DATE		DATE	